THAT WHICH IS CLAIMED IS:

1. In a programmable look-up table (LUT) apparatus, which includes a plurality of programmable data storage cells, each of which produces a cell output signal indicative of the data stored in that cell, and means for normally selecting from all of said cell output signals any one of said cell output signals as a normal output signal on a normal output lead of said look-up table apparatus, said means for normally selecting being responsive to a plurality of first input signals such that each of said first input signals normally controls a respective one of a plurality of successive selection means which collectively comprise said means for selecting, a first said selection means selecting one of two mutually exclusive and collectively exhaustive subsets of said cell output signals, and each succeeding selection means selecting one of two mutually exclusive and collectively exhaustive subsets of the cell output signals selected by the preceding selection means until a final one of said selection means produces said normal output signal on said normal output lead, an improvement for enabling said look-up table (LUT) apparatus to perform a two-bit arithmetic operation comprising:

dividing said LUT apparatus into two equal halves, except for the final selection means, each half comprising half the remaining selection means, half the number of said data storage cells, and half said input signals;

a first means for choosing a selection input for the final selection means in each of said halves to be either a first input signal from the second half

during normal mode, or the carry output from the previous bit operation during an arithmetic mode, the final selection means at the output of the complete LUT apparatus being a second input signal from the second half, and

a second means for connecting the output from the final stage of the first half as the least significant bit output of the two-bit arithmetic operation and using the output of the final stage of the second half as the most significant output bit of the two-bit arithmetic operation during an arithmetic mode while allowing normal selection operation using one of the input signals from the other half during normal mode.

2. The programmable look-up table (LUT) apparatus as claimed in claim 1 further including means to selectively apply either one input signal of the second half or one input signal of the first half as the first input signal to the second half.

3. The programmable look-up table (LUT) apparatus as claimed in claim 1 further including additional logic means connected to each half for generating a carry out for the corresponding bit operation, while simultaneously generating the sum output, using the same memory elements of said LUT.

4. The programmable look-up table (LUT) apparatus as claimed in claim 3 wherein said logic means comprises an exclusive-OR device receiving the outputs from the penultimate selection means of said half as a selection signal for selecting either the

carry-in signal or the second input signal to said half to generate said carry out signal.

5. The programmable look-up table (LUT) apparatus as claimed in claim 1 further including a counting mode of operation wherein a storage element at the output of each half is used to store the result of the previous arithmetic operation for use as an input to said half for counting whenever the counting mode is selected.

6. The programmable look-up table (LUT) apparatus as claimed in claim 1 wherein said first means in each half is a multiplexing means.

7. The programmable look-up table (LUT) apparatus as claimed in claim 6 wherein the select input to said multiplexing means in each half is from a memory.

8. The programmable look-up table (LUT) apparatus as claimed in claim 1 wherein said second means comprises an AND gate.

9. The programmable look-up table (LUT) apparatus as claimed in claim 1 wherein said first means for each half is either the first input signal from the other half during normal mode or the carry output from the lower significant bit operation during arithmetic mode, while the final selection means at the output of the complete LUT apparatus is the XOR of the last selection signal from each half, thereby enabling the use of the LUT as either a single LUT of n inputs or two independent LUTs of n-1 inputs, each in normal

mode, while retaining all the functionality of the arithmetic mode of operation.

10. An electronic and counting unit including an LUT as herein described.

11. The programmable look-up table (LUT) apparatus substantially as herein described with reference to and as illustrated in the accompanying drawings.